switching of signal V_{OUT} and V_{REF} changes the operation of the current mirror as follows.

When signal SB1 is low, the only operational difference between buffers **400** and **500** is that signal V_{OUT} is only inverted twice, because the current mirror remains off. However, when signal SB1 is high in buffer **500**, MOSFET **428** is turned off and MOSFETs **404**, **406** and **420** are turned on, which turns on the current mirror (MOSFETs **406** and **420** are turned on by V_{REF} which passes through MOSFET **404**). Further, when signal V_{OUT} is higher than V_{REF} in buffer **500**, MOSFET **426** is turned off so that no current is passed by the current mirror. Therefore, the current mirror outputs a high signal which is inverted twice and passed to terminal IN. When signal V_{OUT} is lower than V_{REF} in buffer **500**, MOSFET **426** is turned on and the current mirror outputs a low signal which is inverted twice and passed to terminal IN.

Thus, a programmable logic device having a programmable logic circuit to select any one of several different logic drivers is provided. One skilled in the art will appreciate that the present invention can be practiced by other than the described embodiment, which is presented for purposes of illustration and not of limitation. For example, while the detailed schematics of the input buffers and output buffer show specific configurations of n-channel and p-channel MOSFETs, the principles of the present invention may be practiced using n-channel MOSFETs for p-channel MOSFETs and vice versa with a slight adjustment of signal inputs and outputs. Thus, the present invention is limited only by the claims which follow.

What is claimed is:

1. A programmable input/output device for coupling a programmable logic device (PLD) to external circuitry, the input/output device comprising:

an input/output pad;

an output buffer adapted to receive output signals from the PLD, the output buffer modifying the output signals and being coupled to the input/output pad;

an input buffer adapted to receive input signals from the input/output pad and from the output buffer, the input buffer modifying the input signals and being coupled to the PLD to provide the PLD with the modified input signals; and

a plurality of logic standards; and

a plurality of programmable logic elements that select a logic standard from said plurality of logic standards with which the output buffer and the input buffer respectively modify the output and input signals.

2. The programmable input/output device of claim **1**, wherein the plurality of programmable logic elements comprises:

a first programmable logic element coupled to the output buffer and the input buffer; and

a second programmable logic element coupled to the output buffer.

3. The programmable input/output device of claim **2**, wherein the plurality of programmable logic elements are SRAM elements.

4. The programmable input/output device of claim **2**, wherein the plurality of programmable logic elements are EPROM elements.

5. The programmable input/output device of claim **2**, wherein the plurality of programmable logic elements are EEPROM elements.

6. The programmable input/output device of claim **2**, wherein the plurality of programmable logic elements are antifuse elements.

7. The programmable input/output device of claim **2**, wherein the plurality of programmable logic elements are elements from the group of SRAM, EPROM, EEPROM, and antifuse elements.

8. The programmable input/output device of claim **1**, wherein the input/output device provides signal modification in accordance with TTL standards.

9. The programmable input/output device of claim **1**, wherein the input/output device provides signal modification in accordance with CMOS logic standards.

10. The programmable input/output device of claim **1**, wherein the input/output device provides signal modification in accordance with open drain logic standards.

11. The programmable input/output device of claim **1**, wherein the input/output device provides signal modification in accordance with GTL standards.

12. The programmable input/output device of claim **1**, wherein the input/output device provides signal modification in accordance with HSTL standards.

13. The programmable input/output device of claim **12**, wherein the HSTL standard is terminated.

14. The programmable input/output device of claim **12**, wherein the HSTL standard is non-terminated.

15. The programmable input/output device of claim **1**, wherein the input buffer comprises:

a differential amplifier circuit being adapted to receive the input signals;

control circuitry that controls the modification of the input signals in accordance with the standard selected by the plurality of programmable logic elements; and

inversion circuitry that provides the modified input signals to the PLD.

16. The programmable input/output device of claim **15**, wherein the differential amplifier circuit and the control circuit operate in conjunction with each other to provide the modifications of the input signals in accordance with a plurality of logic standards.

17. The programmable input/output device of claim **15**, wherein the differential amplifier circuit and the control circuit operate independent of each other such that the modifications of the input signals are performed by the control circuitry in accordance with a first logic standard and by the differential amplifier circuit in accordance with a second logic standard, the first and second logic standards being selected by the plurality of programmable logic elements.

18. The programmable input/output device of claim **17**, wherein the control circuitry is optimized for speed to provide modification in accordance with the first logic standard at increased speed.

19. The programmable input/output device of claim **17**, wherein the differential amplifier circuit is optimized for speed to provide modification in accordance with the second logic standard at increased speed.

20. A programmable input/output device for coupling a programmable logic device (PLD) to external circuitry, the input/output device comprising:

means for coupling the input/output device to the external circuitry;

means for receiving output signals from the PLD and for modifying the output signals in accordance with a selected logic standard, the means for receiving providing the modified output signals to the means for coupling;

means for modifying input signals received from the means for receiving and the means for coupling in

accordance with the selected logic standard, the means for modifying providing the modified input signals to the PLD; and

means for selecting the selected logic standard from a plurality of logic standards.

21. The programmable input/output device of claim **20**, wherein the means for receiving comprises:

circuitry for modifying the output signals to an appropriate high voltage level in accordance with the selected logic standard if the output signals are logic high signals; and

circuitry for modifying the output signals to an appropriate low voltage level in accordance with the selected logic standard if the output signals are logic low signals.

22. The programmable input/output device of claim **21**, wherein the selected logic standard is TTL, the appropriate high signal is about 2.4 volts, and the appropriate low signal is about 0.4 volts.

23. The programmable input/output device of claim **21**, wherein the selected logic standard is GTL, the appropriate high signal is about 1.2 volts, and the appropriate low signal is about 0.8 volts.

24. The programmable input/output device of claim **21**, wherein the selected logic standard is CMOS, the appropriate high signal is about 3.5 volts, and the appropriate low signal is about 0 volts.

25. The programmable input/output device of claim **21**, wherein the selected logic standard is open drain, the appropriate high signal is determined by external circuitry, and the appropriate low signal is less than about 0.4 volts.

26. The programmable input/output device of claim **21**, wherein the selected logic standard is terminated HSTL, the appropriate high signal is determined by external circuitry, and the appropriate low signal is about equal to the appropriate high signal minus 0.1 volts.

27. The programmable input/output device of claim **21**, wherein the selected logic standard is non-terminated HSTL, the appropriate high signal is about equal to a predetermined reference voltage plus 0.1 volts, and the appropriate low signal is about equal to the predetermined reference voltage minus 0.1 volts.

28. The programmable input/output device of claim **20**, wherein the means for modifying comprises:

a first conversion circuit for converting the input signals in accordance with a first logic standard; and

a second conversion circuit for converting the input signals in accordance with a second logic standard.

29. The programmable input/output device of claim **28**, wherein the first and second conversion circuits are merged into a single conversion circuit.

30. The programmable input/output device of claim **28**, wherein the first and second conversion circuits are substantially independent of each other such that they may be independently optimized for operational speed improvements.

31. A method for providing a programmable logic device (PLD) with the capability of being selectively coupled to external circuitry which operates in accordance with a selected one of a plurality of logic standards, the methods comprising the steps of:

programmably selecting the selected one of a plurality of logic standards;

modifying output signals from the PLD in accordance with the selected logic standard such that high PLD signals correspond to high signals of the selected standard and low PLD signals correspond to low signal of the selected standard;

receiving input signals from an external interface; and

modifying the input signals in accordance with the selected logic standard such that high input signals are converted to high PLD signals and low input signals are converted to low PLD signals.

32. The method of claim **31**, wherein the step of programmably selecting the selected one of a plurality of logic standards selects a logic standard from the group including: TTL, CMOS logic, open drain logic, GTL, terminated HSTL, and non-terminated HSTL.

33. The method of claim **31**, wherein the step of programmably selecting comprises the step of applying a plurality of Select Bits to a plurality of programmable elements.

34. The method of claim **33**, wherein the programmable elements are from the group including: SRAM, EPROM, EEPROM, and anti-fuse elements.

* * * * *